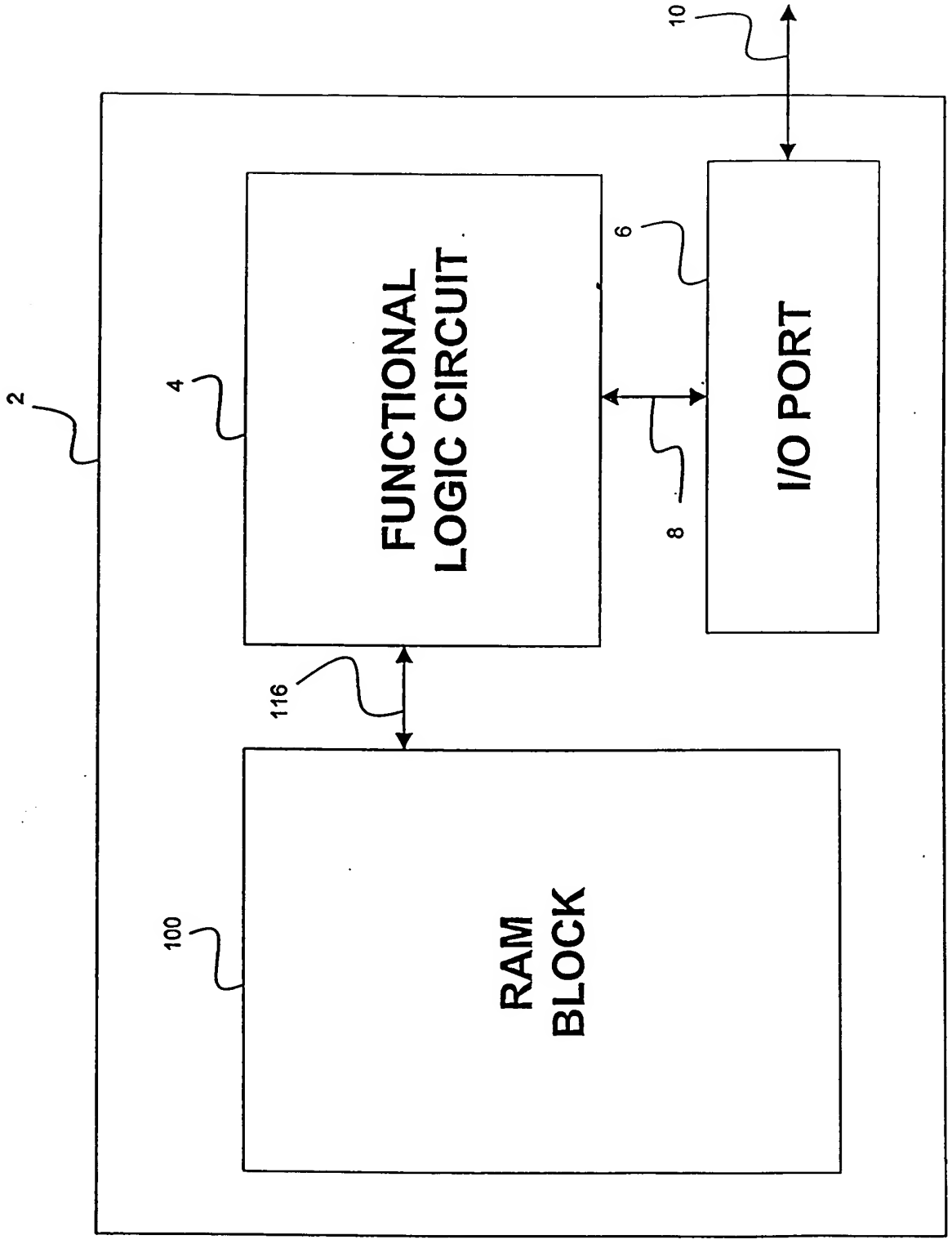

FIG. 1

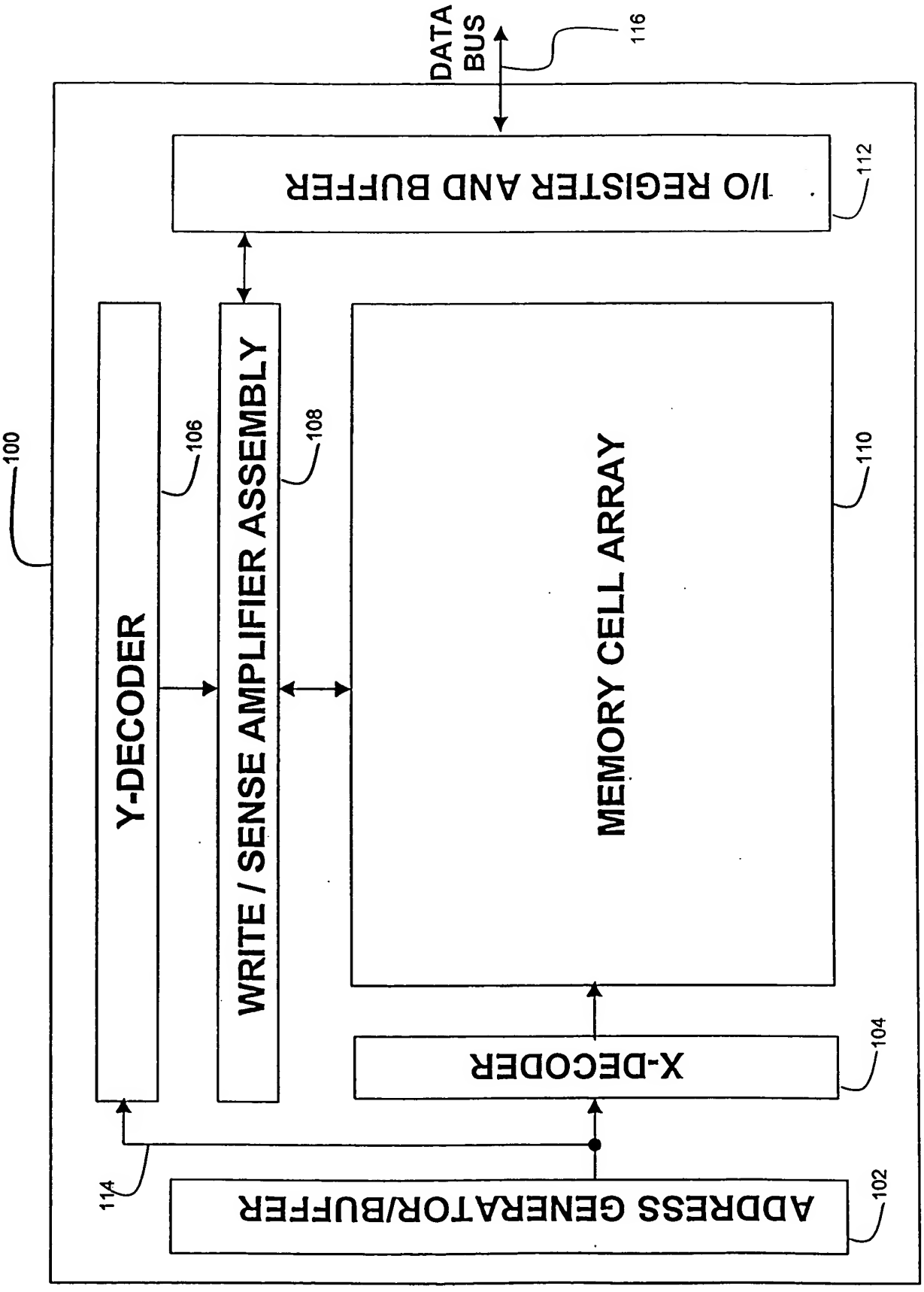
DATA BUS
116
I/O REGISTER AND BUFFER
112
Y-DECODER
106
WRITE / SENSE AMPLIFIER ASSEMBLY
108
MEMORY CELL ARRAY
110
100
X-DECODER
104
ADDRESS GENERATOR/BUFFER
102
114

FIG. 2

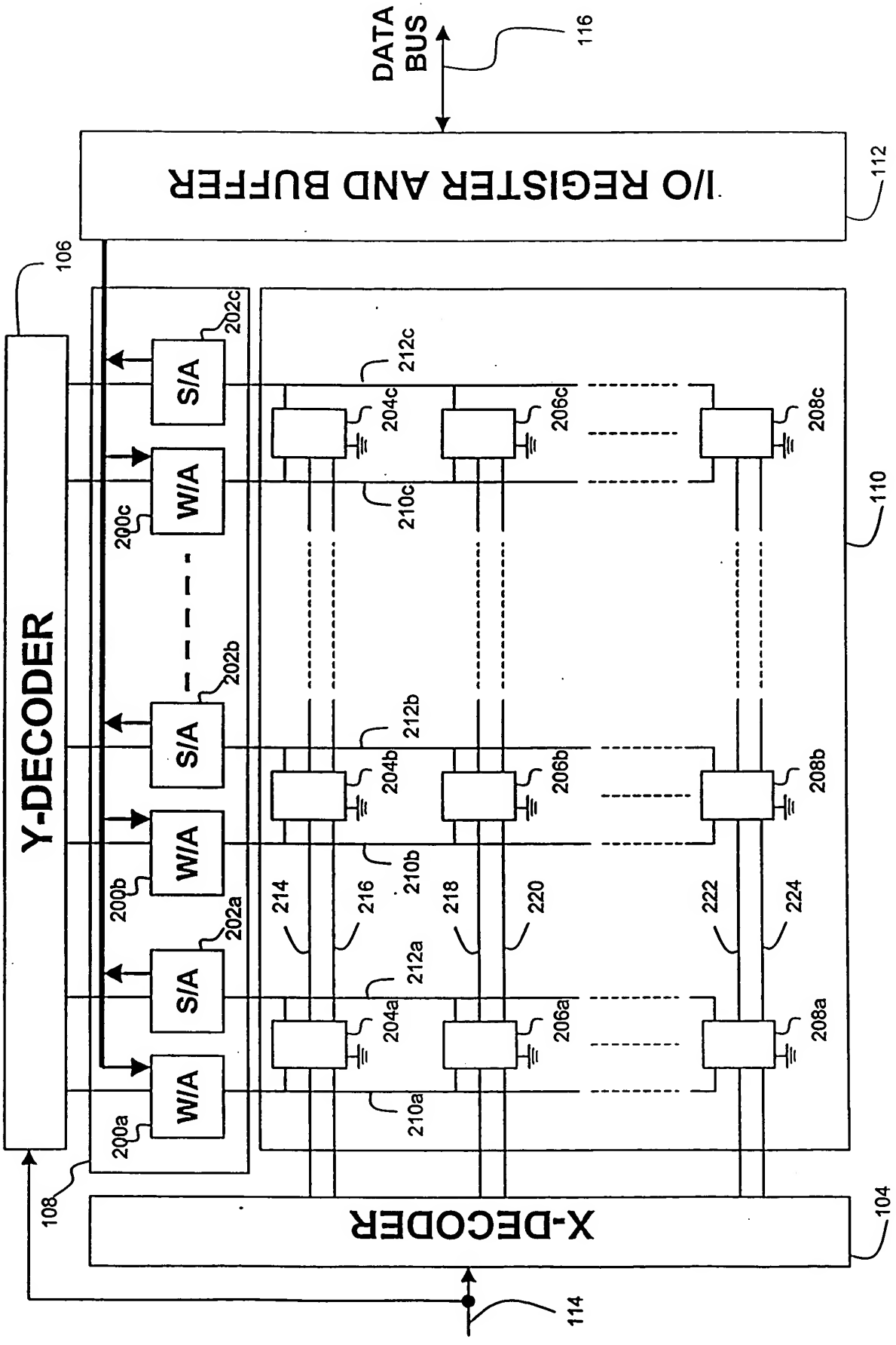
DATA BUS
116
I/O REGISTER AND BUFFER
112
106
Y-DECODER
S/A
W/A
202c
200c
202b
200b
202a
200a
212c
212b
212a
204c
204b
204a
206c
206b
206a
208c
208b
208a
210c
210b
210a
214
216
218
220
222
224
110
108
X-DECODER
104
114

FIG. 3

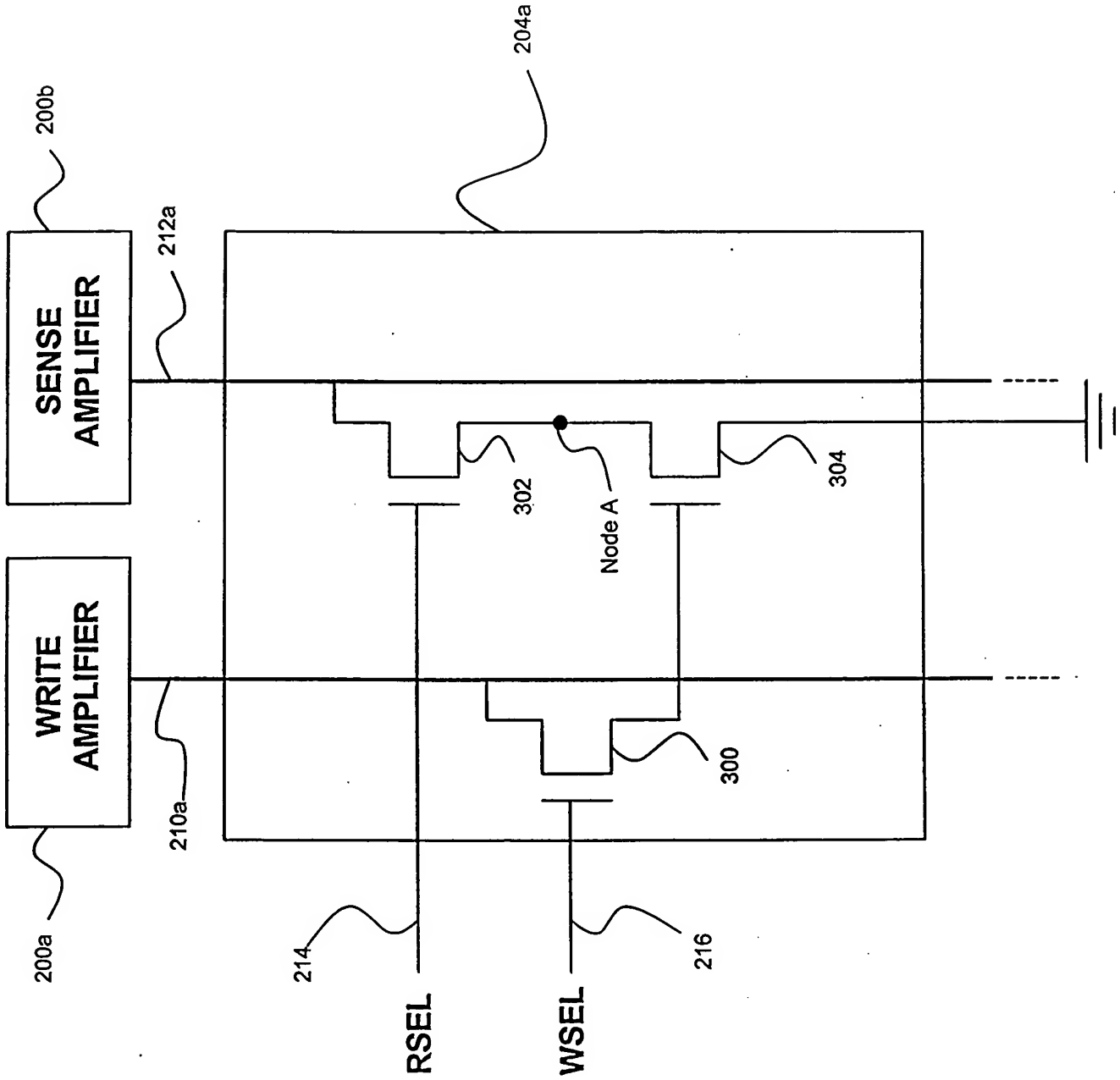
200b
204a
212a
SENSE AMPLIFIER
302
Node A
304
WRITE AMPLIFIER
210a
300
200a
214
216
RSEL
WSEL

FIG. 4

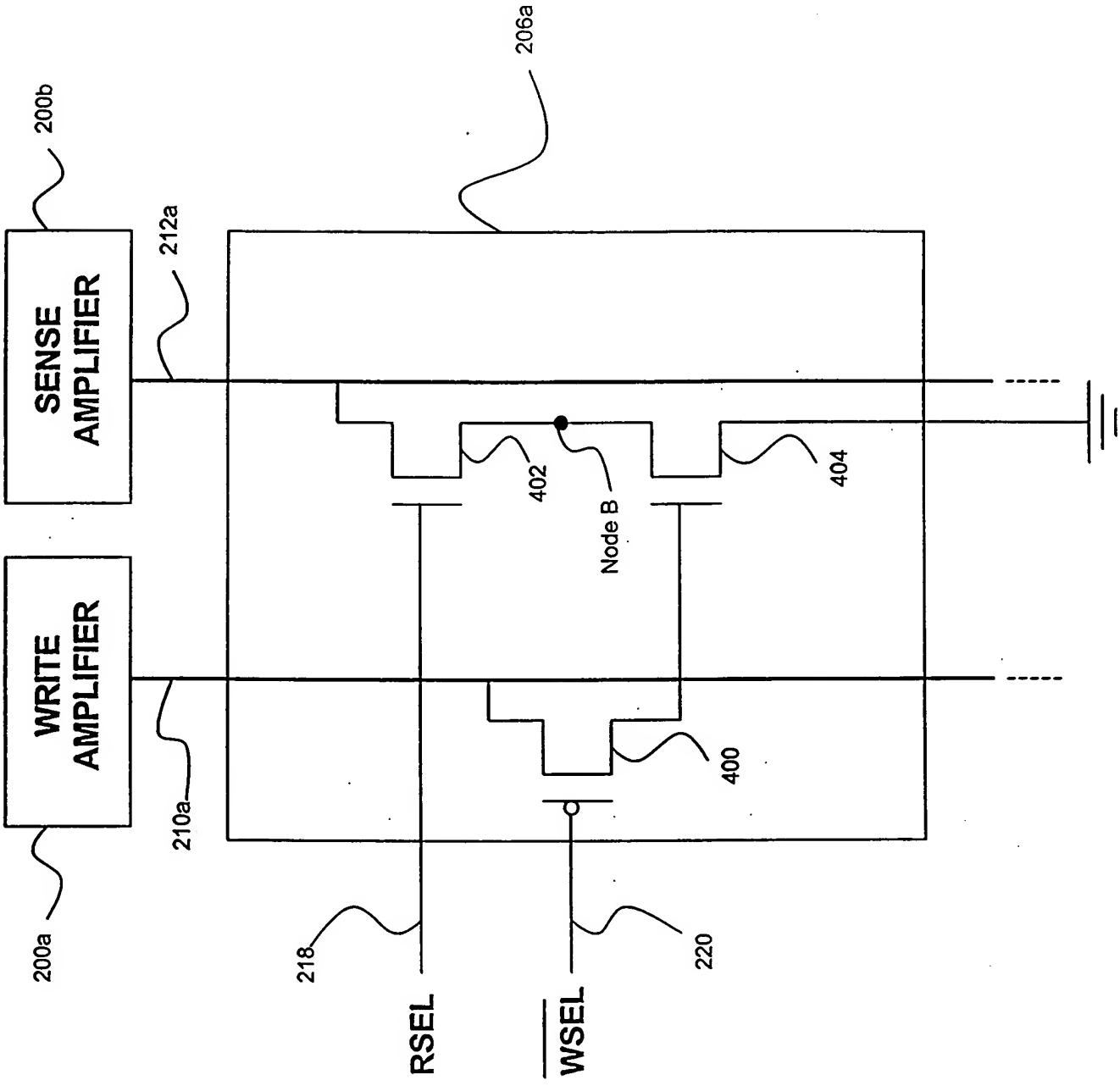
200b
206a
212a
SENSE AMPLIFIER
402
Node B
404
WRITE AMPLIFIER
210a
400
200a
218
220
RSEL
WSEL

FIG. 5

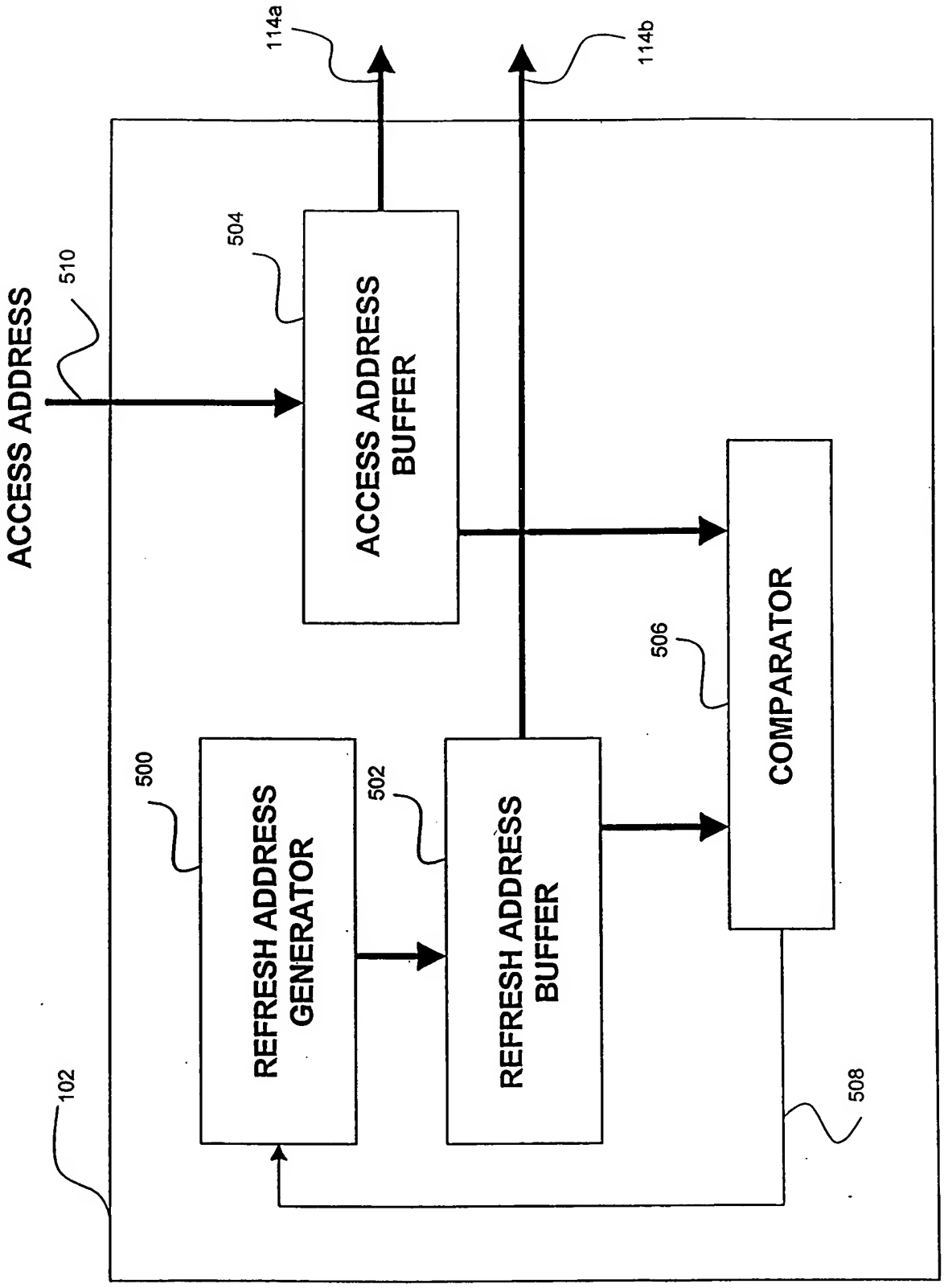
114a
114b
ACCESS ADDRESS
510
504
ACCESS ADDRESS BUFFER
506
COMPARATOR
500
REFRESH ADDRESS GENERATOR
502
REFRESH ADDRESS BUFFER
508
102

FIG. 6

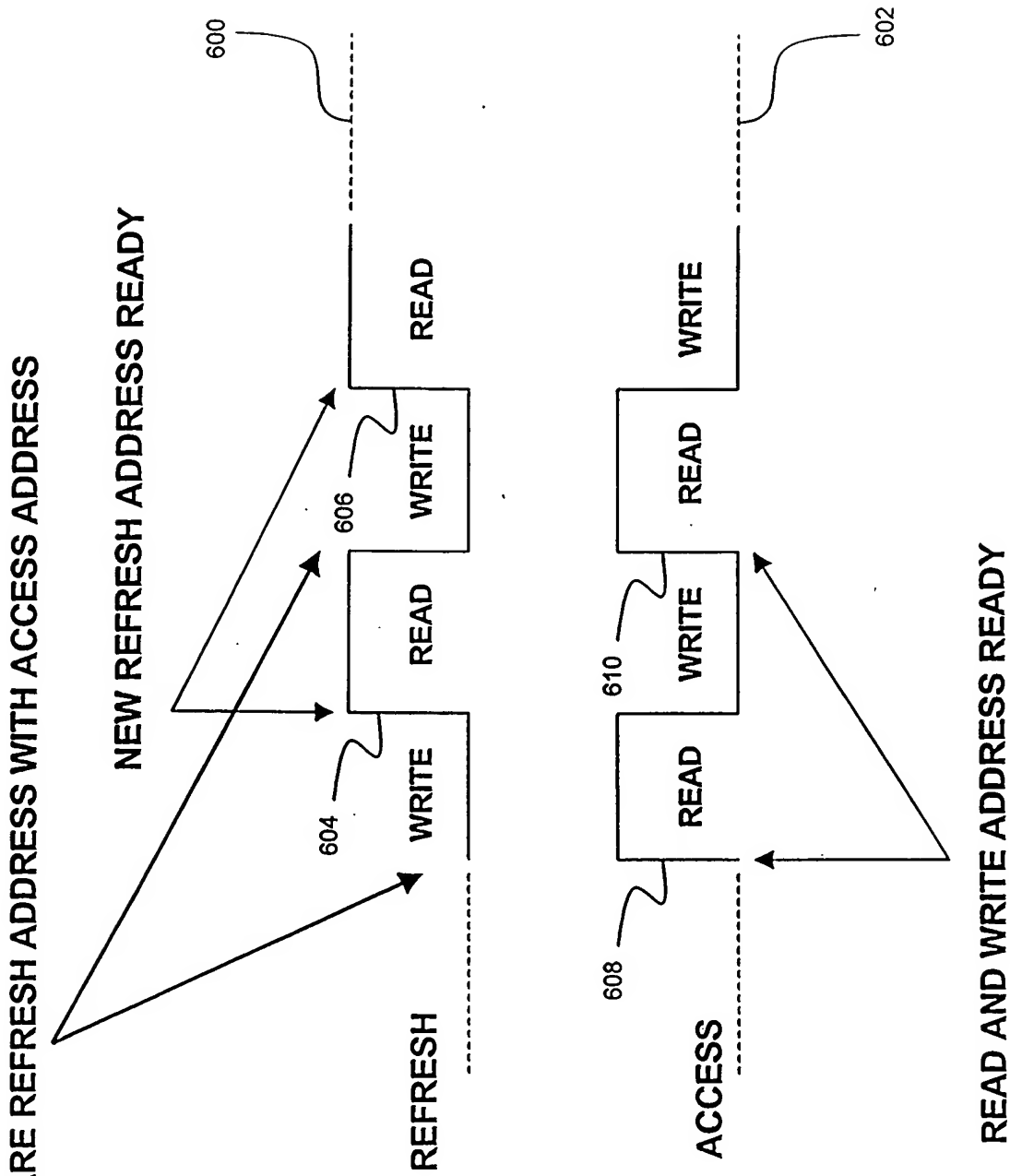
COMPARE REFRESH ADDRESS WITH ACCESS ADDRESS
NEW REFRESH ADDRESS READY
600
602
606
604
610
608
WRITE
READ
WRITE
READ
WRITE
READ
WRITE
READ
REFRESH
ACCESS
READ AND WRITE ADDRESS READY

FIG. 7

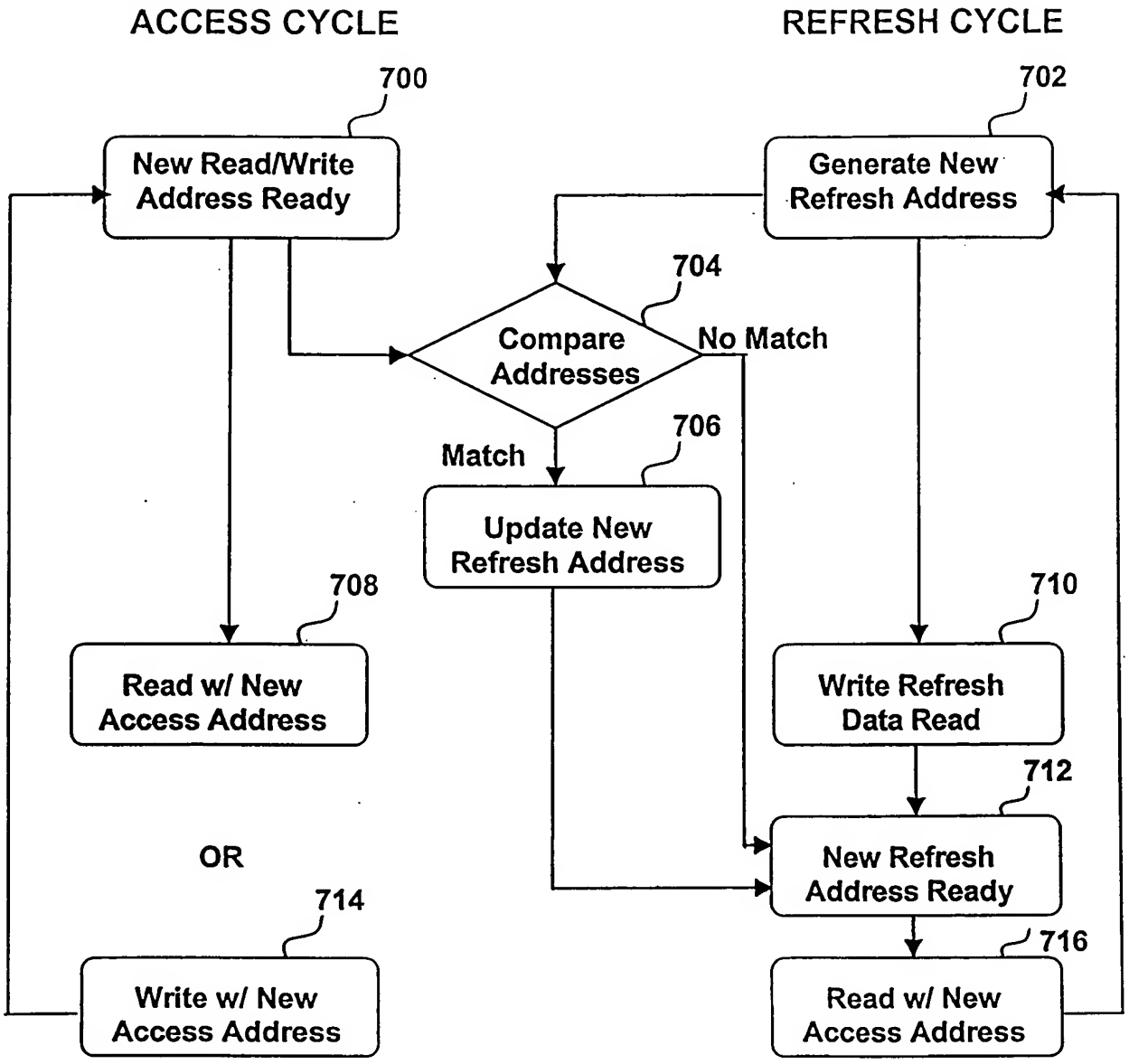
ACCESS CYCLE
REFRESH CYCLE
700
New Read/Write Address Ready
702
Generate New Refresh Address
704
Compare Addresses
No Match
Match
706
Update New Refresh Address
708
Read w/ New Access Address
710
Write Refresh Data Read
712
New Refresh Address Ready
OR
714
Write w/ New Access Address
716
Read w/ New Access Address

FIG. 8